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DESIGN AND DEVELOPMENT OF DUAL OUTPUT DC – DC FORWARD CONVERTER

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ABSTRACT

The purpose of this paper is to implement MOSFET based high precision low size dual output DC-DC forward converter with current mode control operating at a switching frequency of 500KHz. The proposed design also has added feature of over temperature protection. In this design in addition to the voltage feedback the MOSFET current is also sensed which is fed back for faster response. The dual output of +15V and -15V with a output current of 0.75A and a power rating of 22.5W is achieved with the input voltage varying from 18V to 36V.

KEYWORDS: DC-DC Converter, Pulse Width Modulation

INTRODUCTION

Power supply is a system that supplies electric power to the load [1]. There are two broad categories of power supplies[2]:

- Linear regulated power supply
- Switched mode power supply (SMPS)

Of late most of the power supplies are replaced by switching mode power supplies (SMPS) because of the existing disadvantage of the requirement of large size low frequency transformer in linear regulated power supplies [3]. DC-DC converters are a class in switched mode power supplies (SMPS) consisting of switches, energy storage elements, filters and isolation transformers used to convert DC voltage of one level to another with regulation[3], [4].

The purpose of this paper is to implement MOSFET based high precision low size dual output DC-DC forward converter. The main advantage for selecting this topology is that it is used for medium power applications; high switch utilization and number of switching devices are less. In this paper current mode control is used in order to get faster response and the high switching frequency results in reduction in the transformer core size.

METHOD OF CONTROL

The switching converter output voltage is a function of the input voltage, duty cycle and load current as well as converter circuit component values. The output voltage should be constant regardless of variation in input voltage, load current and converter circuit parameter values. Despite variation, it is desired that the output voltage be within a certain limit. The constant output voltage cannot be practically achieved without negative feedback and setting the duty cycle to a single value. The basic methods of controlling the duty cycle to keep the output voltage within the specified limit are:

- Voltage Mode Control
- Current Mode Control

Voltage Mode Control

In voltage mode control, the output voltage is measured and then compared with the reference value (desired output voltage). The error is then processed by the compensation block to generate the next duty cycle value, as shown in

Fig 1[5]. This mode has only one control loop, so it is easy to design and analyze. However, in this control method, any change in the line or the load must be first sensed as an output voltage change and then corrected by the feedback loop. Therefore, the response is slow and the transient response is not favourable.

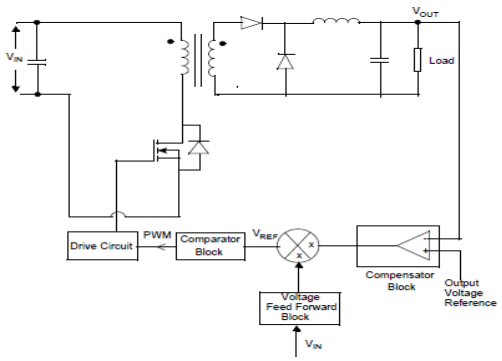

Figure 1: Voltage Mode Control

Current Mode Control

The current mode control technique requires two feedback loops, as shown in Fig 2 [5]. In this mode, two parameters are measured for control purposes. The output voltage is measured at the output capacitor or at the load end (known as remote sensing). The output inductor/primary switch current is also measured. In current mode control, the output voltage is first compared with the reference voltage (desired output voltage). This error is then processed by the compensation block to generate the reference signal for the current loop. This current reference is compared with the measured current. Any error generated by the comparison of the reference generated by the voltage compensation block and the actual current drawn from the input is processed by the current compensation block. This generates the required duty cycle to maintain the output voltage within the specified limit. As current mode control senses the circuit current, any change in output load current or the input voltage can be corrected before it affects the output voltage. Sensing the input current, which depends on input voltage, provides the inherent feed-forward feature. It also improves step load response and transient response because of the inner current loop.

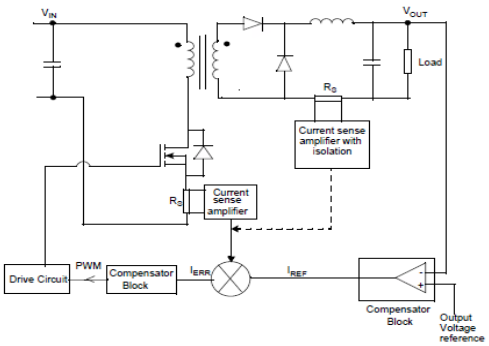

Figure 2: Current Mode Control

Control Circuit Model of CMC Forward Converter

Fig. 3 shows a basic configuration of the CMC forward converter [6]. Where, V_{in} is the input voltage and R_L is a load resistance. In current mode control (CMC) forward converter, a flip-flop is set by a constant cycle clock and a switch is turned on. After the switch is turned on, the switching current i_S begins to rise like a trapezoid wave. An error amplifier outputs a control signal V_c obtained by amplifying the error between a detected voltage of an output voltage V_o and a reference voltage V_{ref}. The value of the control signal V_c minus a ramp signal i_R is compared with the switching current i_S

in a comparator. The ramp signal i_R is employed to improve the control stability. When the switching current i_S reaches this value, the flip-flop is reset by the output signal from the comparator and the switch is turned off. Thus, an on duty D is determined. A voltage conversion is done by repeating the above-mentioned operation. Modeling of CMC forward converter shown in Fig. 3 is obtained based on the following assumptions:

a) The switching transistor, the inductor L, and the output capacitor C are ideal.

b) The switching transistor has no delay time of the switching.

c) The inductor current is continuous.

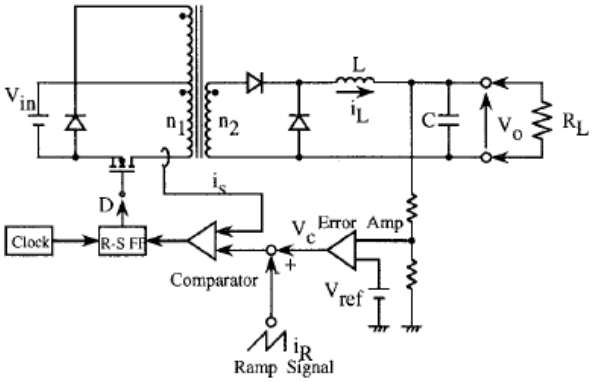

Figure 3: Configuration of CMC Forward Converter

DESIGN CONSIDERATIONS

The block diagram in Fig 4 shows the dual output DC-DC Converter which is designed to operate at a switching frequency of 500 KHz with input being allowed to vary from 18V to 36V. It has input to output isolation provided by transformer TX2. Closed loop control is provided by a voltage feedback and current sense circuits. Voltage feedback is provided by an optocoupler and current is sensed using current sense transformer for faster response. The design also provides with over temperature protection circuit provided by Quad Comparator LM139.

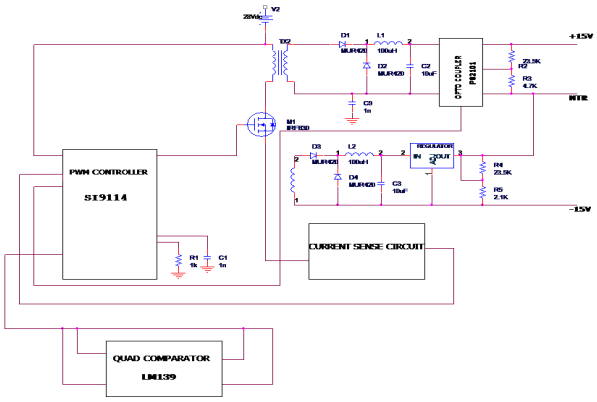

Figure 4: Block Diagram of Dual Output DC-DC Converter

The equivalent circuit of the forward DC-DC Converter is as shown in Fig 5. It consists of high frequency switchmode PWM controller Si9114A which drives the MOSFET and is designed to operate at a frequency of 500 KHz. For voltage feedback an optocoupler PS2101 used, current sense transformer TX1 is used to sense the MOSFET current which is fed back to the current sense input of the PWM controller for faster response. A LDO regulator is used at the output of the power stage. An over temperature protection circuit is provided by the Quad Comparator LM139 using a thermistor.

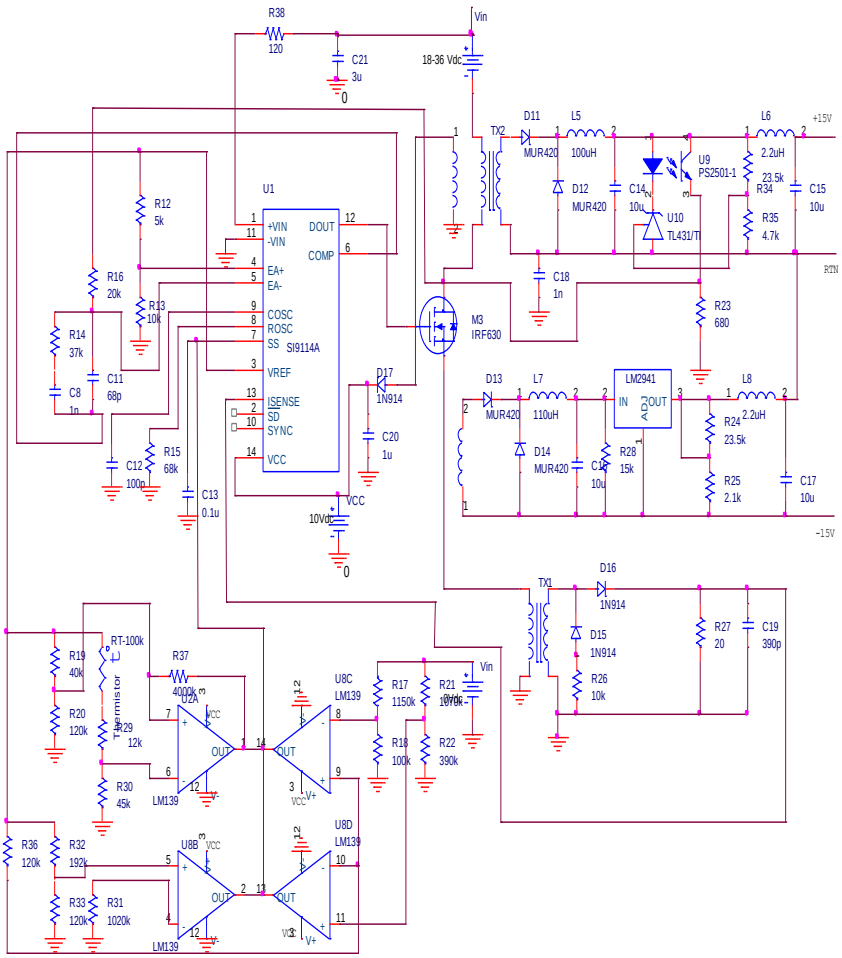

Figure 5: Equivalent Circuit of Dual Output DC-DC Forward Converter

COMPONENT DETAILS

High-Frequency Switch mode Controller Si9114A

The PWM Controller used in the design is Si9114A. The Si9114A is a BiC/DMOS current-mode pulse width modulation (PWM) controller IC for high-frequency DC-DC converters. Single-ended topologies (forward and flyback) can be implemented at frequencies up to 1 MHz. The oscillator has an internal divide-by-two that limits the duty ratio to 50%. An oscillator sync output allows converters to be synchronized in phase as well as in frequency, in a master/slave configuration [7]. Other features include a 1.5% accurate voltage reference, error amplifier, shutdown logic control, soft-start and under voltage lockout circuits. Functional block diagram of Si9114A is as shown in Fig 6.

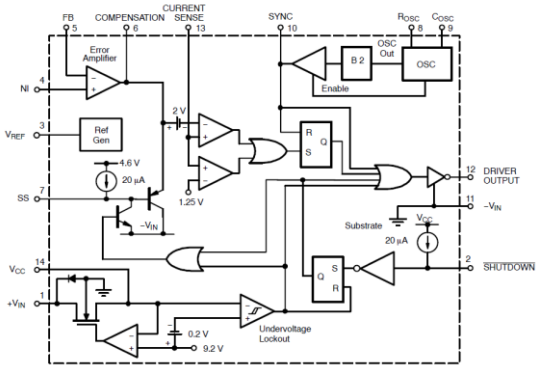

Figure 6: Functional Block Diagram of Si9114A

Low power low offset Quad Comparator LM139

Quad Comparator is mainly used for over temperature protection, wherein if the temperature crosses certain limit output of the quad comparator goes low. And also if input voltage goes below certain level, output of quad comparator goes low. In this design, all four comparator are ANDed and given as input to the soft start of the PWM controller Si9114A, such that if even one of the outputs of any one of the four comparators goes low, input to the soft start is held low.

Calculation of Switching Frequency

T_{ON} =(1.025 X R_T * C_T) / 8

T_{OFF} =5 * Rql X C_T ; Where Rql = 25 ohms

F_{OSC} =1/2(T_{ON}+ T_{OFF})

Selecting R_T=68K ohms & C_T =100pF and

Substituting these values in the above equations yields:

T_{ON} =(1.025 * R_T * C_T) / 8

T_{ON} =(1.025 * 68 * 10^3 * 100 * 10^{-12}) / 8

T_{ON} = 0.87125 * 10^{-6} sec

T_{OFF} =5 * Rql * C_T; Where Rql = 25 ohms

T_{OFF} =5 * 25 * 100 * 10^{-12}

T_{OFF} =0.0125 *X 10^{-6} sec

F_{OSC} =1/2(T_{ON}+ T_{OFF})

F_{OSC} =1/2((0.87125 * 10^{-6})+ (0.0125* 10^{-6}))

F_{OSC} =565.77 * 10^3 Hz

F_{OSC} =565.77K Hz

Design of Capacitor and Inductor for Forward Converter

Pout = Vout*Io = 15*0.75= 11.25W

Pin = Pout /eff = 11.25/0.8 =14.0625 W

Idc = Pin /Vin = 14.0625/18= 0.7812A

I_A = Pin /(Vin*d) = 14.0625/(18*0.4929) = 1.5625A

I_{RMS} = IA/2 = 1.5625/2 = 0.78125A

V_{RIPPLE} = 20mV

C_{MIN} = I_{RMS} /(8*f_{SW}* V_{RIPPLE})= 0.78125/(8*500*10^3*20*10^{-3})= 9.8uf

Practically C of value larger than the calculated value is chosen. Hence C=10uF

V_L= Ldi/dt

$V_L = E_{IN} - E_{OUT} - E_{SW} = 28-15-1.5 = 11.5V$

$t_{off} = 1/(2*fsw) = 1/(2*500*103)$

$\Delta I_l = 0.1*Iout = 0.1*0.75 = 0.075A$

$L = (V_L * t_{off}) / \Delta I_l = (11.5*1*10\text{-}6)/0.075 = 153.3uH$

Practically inductance of lower value than the calculated value is chosen. Hence L= 100uH to 110uH.

Design of Transformer Turns for Transformer TX2

Np=(Vmin*tonmax)/(Bmax*Aeff)=(18*1*10-6)/(100*10-3*24.5*10-6) =7.3=7turns

Vsec = (Vout + VLoss)/Dmax = (15+1)/0.5 = 32V

Turns Ratio = TR= Vmin/ Vsec = 18/32 = 0.5625

Ns = Np /TR = 7/0.5625 = 12.44 = 12turns

Calculation of Sense Resistor for Current Sensing

Ip=(Vin * ton)/ Lmag +Io*(Ns /Np)= (18*0.871258*10-6)/(35*10^{-6})+ 0.75(12/5) =2.24807A

Is=Ip*(Np1/Ns1)=2.24807*(1/100)= 0.0224807A=22.4807mA

Isd= (Vin * ton)/ Lmags=(18*0.871258*10^{-6})/ (7.94*10^{-3})=1.95mA

Rsense=Vcontrol/Is=1.25/0.0224807=55.6032Ω=50Ω

Vs=Is * Rsense+ Vfwd = (0.0224807*55.6032)+0.7=1.9499V

Lmag = primary magnetizing inductance of the main power transformer (not current sense transformer) [8].

Ns = secondary turns of main power transformer.

Np = primary turns of main power transformer.

Ton = on time of PWM modulator

Np1 = primary turns of current sense transformer, usually 1.

Ns1 = secondary turns of current sense transformer, usually a number between 50 and 100.

Lmags = secondary magnetizing inductance of the current sense transformer.

Vfwd = forward voltage drop of rectifying diode D1.

SIMULATION AND RESULTS

The simulation is carried out using ORCAD PSPICE. Fig.7 shows the simulation circuit diagram of the basic buck converter consisting of calculated values of L and C with L=100µH and C=10µF, diode MUR420 and MOSFET IRF 630 is used as switch with duty cycle of 50% with the input voltage V_{IN} = 28V represented by V_3.

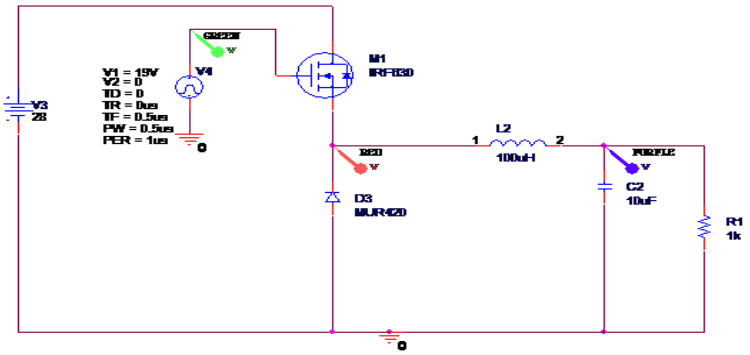

Figure 7: Simulation of Basic Buck Converter

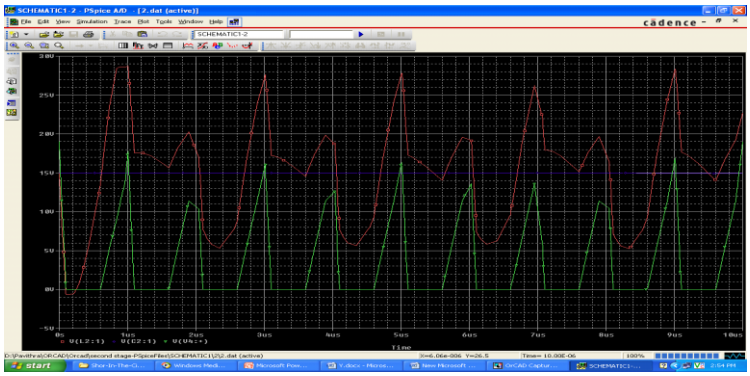

Figure 8: Simulation Result of Basic Buck Converter

Fig 8 shows the simulation result of the basic buck converter shown in Fig.6 and is observed that simulation results in output voltage of 15V represented by the colour purple in Fig8. Waveforms in colour green are the pulses to the MOSFET and in red are the drain waveform of the MOSFET IRF630

Fig 9 shows simulation circuit diagram of Quad comparator LM139 the main purpose of which is over temperature protection. This consists of four comparators whose outputs are ANDed to obtain the final output. Each comparator functions for one of the below mentioned conditions

- If temperature rises beyond 120^{o}C, output of LM139 goes low
- If input voltage, Vin, drops below 15V, output of LM139 goes low
- If voltage Vref below 2.2V, output of LM139 goes low
- If input voltage Vin exceeds 50V, output of LM139 goes low

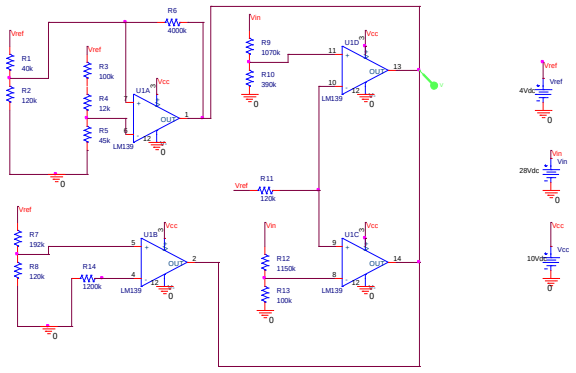

Figure 9: Simulation of Quad Comparator LM139

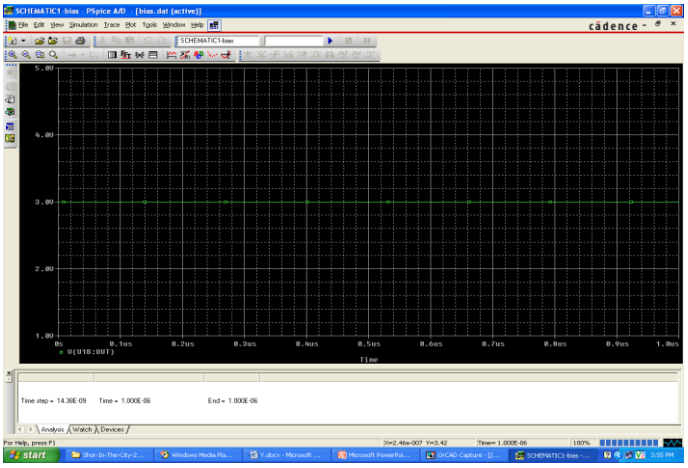

Figure 10: Simulation of Quad Comparator LM139

Fig 10 shows the simulation result of Quad comparator LM139 simulated with input Vin = 28V, Vref=4V, Vcc=10V. Under normal operating conditions it results in output voltage of 3V as shown by colour green in Fig.9 else if even one or all of output goes low , final output goes low .

EXPERIMENTAL SETUP OF FORWARD CONVERTER

The experimental setup of the DC-DC converter on a general purpose PCB is as shown in Fig 11. It consists of Si9114A high frequency current mode control PWM controller for generation of switching pulses at 500 KHz fed to the gate of the MOSFET IRF630. It also consists of low power Quad comparator for the purpose of protection against over temperature. It also consists of isolation transformer, capacitors, Inductors, current sense transformer and current sense resistor used to sense the MOSFET current.

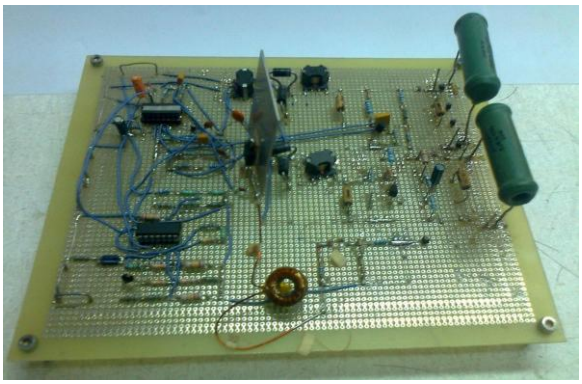

Figure 11: Experimental Setup of Forward Converter

Voltage across two channels at different input voltages under no load condition is measured and tabulated in Table 1. Results obtained for no load condition is found to be satisfied and in good agreement with the expected result

Table 1: Output Voltage across two Channels under No Load Condition

Input Voltage(v)	Output Voltage1(v)	Output Voltage2(V)
18	15.019	-15.034
20	15.019	-15.034
22	15.020	-15.036
24	15.021	-15.038
28	15.022	-15.038
30	15.022	-15.040
36	15.023	-15.043

Table.2 shows the output voltage at channel 1 and 2 for an input voltage of 18V and different load conditions and output is found to be varying for various load condition as the test is carried out in open loop condition. However testing in close loop condition will eliminate the above mentioned problem.

Table 2: Output Voltage Across 2 Channels Under Open Loop Load Condition for Different Loads and V_{IN}=18V

Different Loads	Output Voltage1(v)	Output Voltage2(V)
Full Load=20Ω	+14.186	-14.090
Half Load=40Ω	+14.287	-14.203
20% Load=100Ω	+14.886	-14.794

Table 3 shows the output voltage at channel 1 and 2 for full load and for different input voltages and output is found to be varying for various input voltages as the test is carried out in open loop condition

Table 3: Output Voltage Across 2 Channels Under Open Loop Load Condition for Different Input Voltage and Full Load 20Ω

Input Voltage(v)	Output Voltage1(v)	Output voltage2(V)
18V	+14.186	-14.090
28V	+14.287	-14.203
36V	+14.886	-14.794

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Circuit Waveforms at No Load: Fig 12 shows the ramp voltage waveform of oscillator across C_{OSC} terminal (pin no: 9 of Si9114A) operating at approximately 500 KHz under no load condition. It is similar to the expected waveform except for the switching frequency which should have been 500 KHz but is operating at 454 KHz.

Figure 12: Ramp Voltage Across C_{OSC} at No Load

Figure 13: Gate Waveform at No Load

Fig 13 shows the gate wave form and Fig.14 shows the drain waveform of the switch i.e. MOSFET IRF 630 under no load condition. It is similar to the expected waveform except for noise in the waveform due to operation of the circuit at a switching frequency of 500 KHz and absence of proper grounding for such high switching frequency operation.

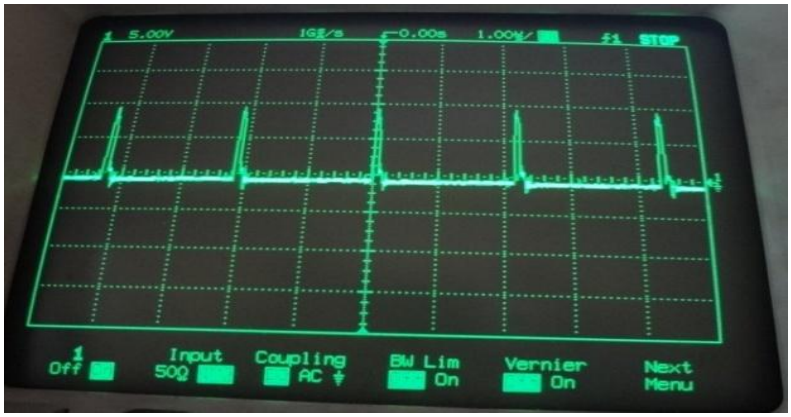

Figure 14: Drain Waveform at No Load

Circuit Waveforms under Load Condition: Fig 15 shows the ramp voltage waveform of oscillator across C_{OSC} terminal (pin no: 9 of Si9114A) operating at approximately 500 KHz under full load condition i.e. 20Ω operating with VIN= 18V.It is similar to the expected waveform except for the switching frequency which should have been 500 KHz but is operating at 454 KHz.

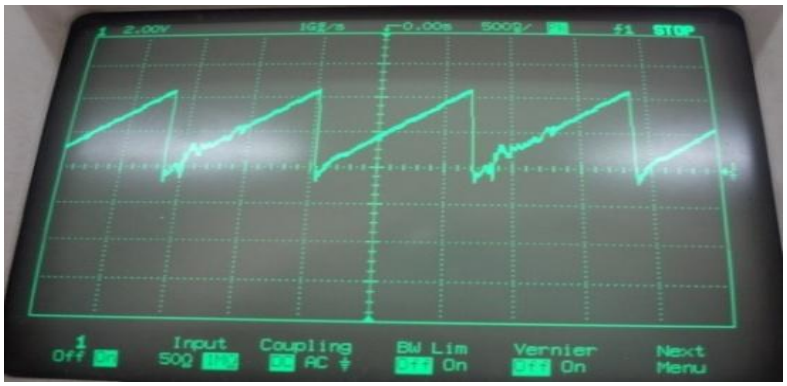

Figure 15: Ramp Voltage Across COSC Under Load Condition

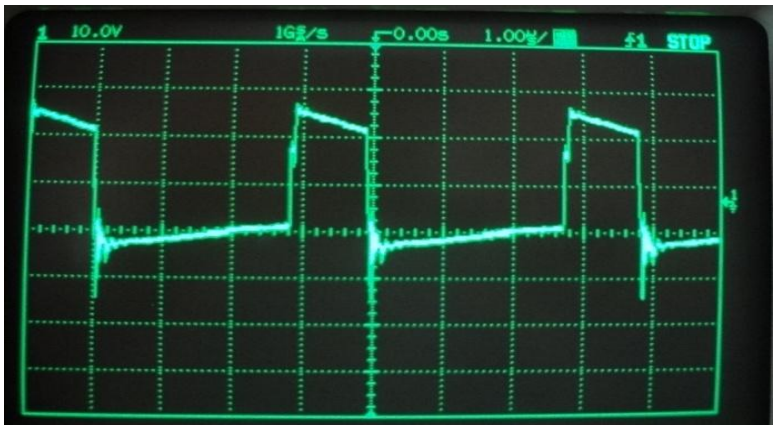

Figure 16: Gate Waveform Under Load Condition

Fig 16 shows the output pulse of the PWM controller (pin no: 10 of Si9114A) at full load with V_{IN}= 18V operating at approximately 500 KHz. Duty cycle was observed to be 34%.

Fig 17 shows the drain waveform of the switch i.e. MOSFET IRF 630 under full load condition and V_{IN}= 18V. It is similar to expected waveform except for certain amount of noise present in the waveform due high switching frequency and inappropriate grounding.

Figure 17: Drain Waveform under Load Condition

Switching frequency can be changed from 454 KHz to 500 KHz by connecting a pot in series with the R_T terminal in the PWM controller and suitably adjusting it. And noise due to high switching frequency can significantly reduced by providing proper grounding facilities.

CONCLUSIONS

In this paper an attempt is made to develop miniature size 22.5W Current mode dual output forward converters. The implementation of 22.5W dual output DC-DC converter includes current mode PWM (pulse width modulation) controller Si 9114 A. This will control the gating pulses to the MOSFET at 500 KHz switching frequency in order to get the regulated output. Over voltage protection is provided by optocoupler PS 2101, and temperature sense protection is provided by Quad comparator LM139.It consists of two control loops for current control and over voltage protection. To check the feasibility of design, converter PCB has undergone various tests like electrical test, synchronization check, line load transient and thermal test. It is found to be in good agreement with the theoretical and practical results. The converter is found to be operating suitably well under no load condition and open loop for load condition.

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